
CES White Paper on AFDX

(Avionics Full Duplex Switched Ethernet)

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REFERENCES

- REF [1]: AFDX End System detailed functional specification (DFS), Ref L42D1515045801
- REF [2]: AFDX Switch detailed functional specification (Switch DFS), Ref L42D15155051901
- REF [3]: AFDX Specification for Test Facility (STF) Ref 769.0601/01, issue 2.0 (11/19/01)
- REF [4]: Specification Technique interne du module Phenicia (STM), Ref, SF_984_STM_Phenicia
- REF [5]: Arinc 664 ADN(Aircraft data Network) communications
- REF[6]: Arinc 653 Avionics application software standard interface
- REF [7]: CES AFDX FPGA technical specifications rel 1.2 (08/08/02)
- REF [8]]: AFDX Software specification, Ref 5354_PSS, issue1.12 (08/26/02)
- REF [9]: AFDX5354 API reference guide
- REF [10]: IEEE Standard 802.3 1998 Edition

GLOSSARY

AFDX:	<i>Avionics Full Duplex Switched Ethernet.</i>
APEX:	<i>Application Executive</i> , as specified in [ARINC653].
API:	<i>Application Programming Interface</i> : functions to interface the AFDX cards and control all its capabilities.
End-System:	An active AFDX client, connected to an AFDX Network to communicate with other clients respecting AFDX rules is called an <i>End-System</i> . It is the subsystem part which must be embedded in each avionics equipment connected to the AFDX network to communicate with the other AFDX clients.
BAG	<i>Bandwidth Allocation Gap</i> : minimal gap between sending time of two consecutive frames for a VL.
CRC:	<i>Cyclic Redundancy Check</i> : result of a logical formula applied to a data flow to control the coherency and validate the transmission.
CSR:	<i>Control and Status Registers.</i>
FCS:	<i>Frame Check Sequence</i> : IEEE 802.3 like frame CRC in the AFDX frames.
FE-FPGA:	Front-end programmable logic chip embedded on the CES MFCC 8443 product to drive the electrical interfaces located on the electrical adaptor (<i>nose</i>)
Frame:	The AFDX protocol is based on the IEEE 802.3 <i>frame</i> principle: this is the minimum information unit transferred in an AFDX link, including protocol encapsulation informations.
GCD:	<i>Greatest Common Divisor.</i>
IFG:	<i>Inter-Frame Gap</i> is the minimum period between the last bit of a frame and the first bit of the next one in the physical link. In IEEE 802.3 format, the minimum IFG is of 12 bytes.
IMA:	<i>Integrated Modular Avionics.</i>
LCM:	<i>Least Common Multiple</i>
MAC:	<i>Medium Access Control.</i>
Message:	a <i>message</i> is a user contiguous set of data transferred on AFDX link in one time.
MFCC:	<i>Multi-Function Computing Core</i> : CES PowerPC based board in PMC format, with adaptable I/O interfaces capabilities.
Network:	To avoid confusion between <i>AFDX Port</i> and <i>Physical Port</i> , the last are also called <i>Network</i> in CES AFDX products (see <i>Port</i> definitions).
Nose:	Removable electrical adaptor, connected to the PMC computing core, to drive all electrical interfaces for AFDX I/O.
OS:	<i>Operating System</i> in the CES 5354 product, a LynxOS operating system is embedded to manage the AFDX firmware.
Port:	In the AFDX domain, 4 different entities are called <i>Port</i> : <ol style="list-style-type: none"> the 2 physical redundant links of an AFDX are also called <i>Physical port</i> and names <i>Port A/Port B</i>, or <i>Port red/Port blue</i>. To avoid ambiguous indications, these ports are renamed <i>Network A/ Network B</i> in the CES AFDX products. the <i>AFDX Port</i>, specified in [AFDX01]. These ports defines the user access rules to AFDX data transmission channels (VLs). This is the communication access connection for AFDX user's applications. <i>UDP port</i>, specified in [RFC768] <i>APEX Port</i>, specified in [ARINC653]. These ports are particular AFDX Ports.
QoS:	<i>Quality of Service</i> : network and protocols rules implemented to guarantee communication characteristic values, such as jitter, minimum bandwidth, maximum latency, medium access time guaranty, predictable transmission time, etc.
Rx:	Abbreviation for <i>Reception</i> .
SAP:	<i>Service Access Point</i> : this is a particular <i>AFDX Port</i> for low-level applications, for frame transmission instead of highest level messages.
Skew:	time difference in the arrival of redundant frame copies for both networks.
SN:	<i>Sequence Number</i> : this a byte added to the AFDX frame payload to manage the redundancy.
Tx:	Abbreviation for <i>Transmission</i>
VL:	<i>Virtual Link</i> : the communication channels used to transfer user's data from an End-System to one or more End-Systems, across the switched AFDX network.

1.0 AFDX: Inception and Background

During the 90s, Airbus has performed a series of technology programs in the context of the A380 project. The goal was to assess which newest technology in various domains (databus communication, flight control, power management, structure) would be the most beneficial for a new generation of aircraft like the A380 (performance, availability, risk and cost). As far as databus communication is concerned, Airbus' goal was to move away from ARINC429 bus in considering several drivers: Cost, bus performance, Flexibility, Applicability.

- Cost covers NRE, RC but also certification, Operation, logistics
- Bus performance considers throughput but also latency, quality of service
- Flexibility must be considered in term of design, maintenance and evolution
- Applicability had to be addressed in the specific context of civil aircraft/avionics requirements

A first consideration was the adoption of other avionics bus e.g. ARINC629 but later on the focus was given on bus technology coming from the telecommunications with a special interest for Ethernet.

In general, commercial buses offer a good ratio performance versus cost with a high degree of technology maturity, the issue being to assess the extra cost to make them applicable to civil aerospace requirements. The maturity, the experience across market, the growth potential and the standardization aspect made the Ethernet the preferred choice of Airbus, and more precisely Airbus decided to make most of the use of Full Duplex (switched) Ethernet. Main advantages were:

- Duplex traffic collision free
- Time bounded latency
- Physical segregation
- Possible mapping of other buses e.g 429, 1553
- Existing integrity and deterministic mechanics adaptable for avionics purpose.

The adoption and modification of the Full Duplex (switched) Ethernet for avionics requirements led to the inception of the AFDX (Avionics Full Duplex Switched Ethernet) protocol specified by Airbus. That will be the first time that a standard network protocol is used extensively to interconnect avionics equipment where multiple emitters and receivers are connected through a switching element.

The Airbus A380 will be the first aircraft to use avionics bus based on AFDX protocol. The AFDX contributes to the IMA (Integrated Modular Avionics) model introducing new possible architecture topologies (Multi function real time computers, Distributed and communication resources) as opposed to the classic avionics model i.e. federated architecture

Table 1 ARINC 429 Performance versus Ethernet Performance

	<i>Speed (Bps)</i>	<i>Frame Size (bit)</i>	<i>Frames per second</i>	<i>Minimum of 429 buses to map 100base Tx</i>
ARINC 429	100 KHz (max)	36	2778	54
ETHERNET	100 Mhz	12304	812	N/A

2.0 Key Concept and Features of AFDX Protocol – Summary

As mentioned previously the AFDX is based on IEEE 802.3 Ethernet and TCP/IP general principles. However it uses specific concept and features to provide secure data transfer with real time constraints, to provide the guarantee of services and determinism required for civil aerospace requirements.

The AFDX specific features and concepts, as part of the protocol itself must provide: specific addressing strategy, transmission timing constraints and redundancy management.

Although, it uses Ethernet media to reduce cost, it is derived from the ATM specifications which, as opposed to a standard ethernet network can address the requirements summarized below.

BANDWIDTH GUARANTEE

Bandwidth control is achieved with advanced queue management and multiple bandwidth use strategies. It introduces the notions of BAGs (Bandwidth Allocation Gap) and of maximum frame size to allocate bandwidth as in ATM CBR (Constant Bit Rate), and UBR (User Bit Rate). This guarantee applies to the key notions of AFDX, the virtual links.

REAL TIME CONTROL

Real-time performance is achieved with latency control in the form of the maximum network transit delay control (end-to-end latency) and also includes an accurate time-stamping logic (specific to CES End Systems).

SERVICE GUARANTEE

Guarantee of services is the feature which made ATM the telecom standard selected against IP for voice, video and binary transmission in the 3G world. The user can select a variety of services and constantly monitor the payload for each of the services, which are concurrently executed.

AFDX will be the first avionics standard to combine the simplicity of Ethernet connections with the richness and security of the ATM protocol and all of this packaged in an avionics environment.

The AFDX network main components are:

- Avionics specific physical layer
- COTS components for MAC layer
- AFDX switches:
 - Active elements addressing 3 functions:
 - to establish a point to point connection between a sender and several receivers via twisted pairs cable
 - to establish communication between subscribers on the network
 - to check frame integrity and bandwidth
 -
- AFDX end systems:
 - The AFDX End system is the subsystem which must be embedded in each avionics systems equipment connected to the network.

3.0 CES Role in AFDX (Examples of Applications using CES AFDX Resources)

As a major player in several world's most advanced programs in military and civil aerospace program, CES has established its expertise and its product concept on COTS modules reusability and scalability developed across 3 vertical markets (Telecom, Aerospace and physics). The AFDX development has benefit from this approach involving trade off analysis and selection of COTS components at the level required (Labs application, flight test)

CES has also a long relationship with EADS Airbus Toulouse participating for the last 15 years in the simulation, flight and ground test programs. This long term relation has facilitated a cooperation with Airbus leading to the development of the AFDX product line covering all the applications requiring development, simulation, test, validation and production control of AFDX connected equipment and switches

Three categories of users / application can be considered:

i. Aircraft Manufacturers

With EADS Airbus Toulouse and EADS Deutschland, the main application is to validate, simulate and integrate AFDX connected elements in the integration simulators, flight test systems and finally training simulators. The requirements range from small volume and low number of channels, portable analyzers and testers to full configuration aircraft-level or flight-worthy test systems.

ii. Aircraft Maintenance

Aircraft test equipment, such as EADS Test and Services ATEC series equipment can easily incorporate the CES AFDX products.

iii. Aircraft Equipment Manufacturers

CES AFDX products allow a fast, efficient and secure integration in the company's test benches, since only COTS hardware and software elements are used.

- Fast integration with powerful and easy to use AFDX starter kits
- Efficient integration
- Secure and low risk (CES AFDX resources are the reference for EADS Airbus Toulouse)

CES has been awarded the contract for the production of AFDX Test Resources to be delivered for simulation and monitoring of the Airbus A380. That covers the hardware integration test bench (BIM), the software integration test bench (BIL) and the System Integration test bench (BIS) as far as ground test system are concerned and for the flight test, the IENA N2 system. (Instrumentation d'Essai de Nouveaux Avions).

The IENA N2 AFDX System is a flight test monitoring/recording VME system composed of 24 AFDX PMCs (48 AFDX channels) with global datation at 1 micro second precision. In this project, CES delivers the full system and subsequently acts as a system integrator.

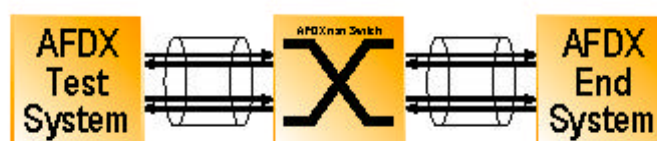
This AFDX products can be combined with the other CES aerospace products e.g. MIL-STD 1553, STANAG 3910 Eurofighter and third party hardware e.g. analog board, master CPU, etc.

Each test application has some typical test requirements. Three typical test cases are summarized below.

SWITCH MONITOR CHANNELS

Links on the switch may be used to monitor AFDX traffic in the system.

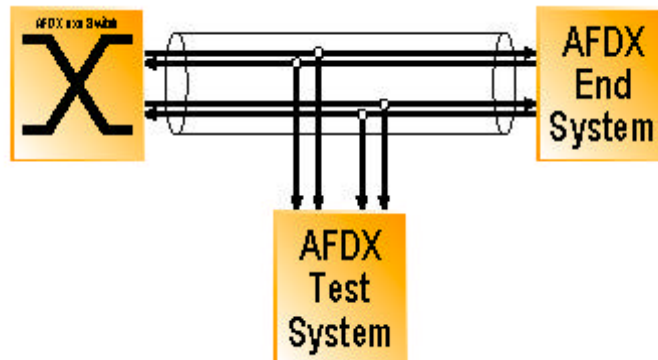
Figure 1 Switch Monitor Channels



TAP

A link may be tapped by a passive adapter (T-piece).

Figure 2 TAP Diagram



RECREM

Test equipment may be inserted into a link data stream. It may modify the data flow on the fly.

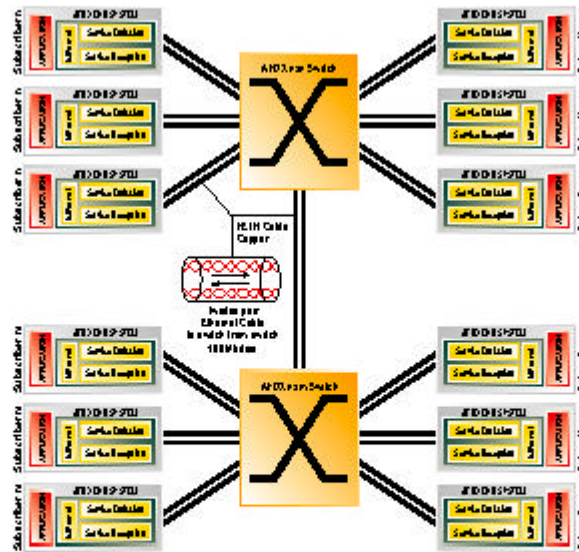
Figure 3 Recrem Diagram



4.0 Topology of an AFDX System

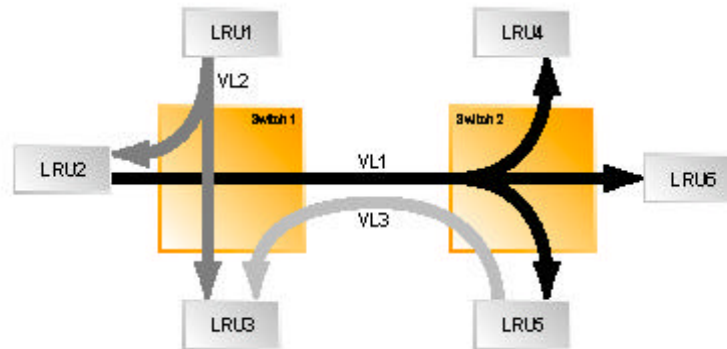
Figure 4 gives a representation of an AFDX system topology. Data are encapsulated in frames whose the structure is defined by the AFDX protocol. Switch and end system are the key components in the AFDX network communication.

Figure 4 AFDX System Topology



4.1 The VL Concept

The most important concept created by AFDX is the VL concept (Virtual Link concept). Such concept allows data transfer separation between one emitter and several receivers. Figure 5 gives a representation of the VL concept (a pipe on the network).

Figure 5 VL Concept

To adapt open protocols such as Ethernet and TCP/IP suites to the strong deterministic demands required by the avionic domain, AFDX defines some particular rules. Some of these specific principles could be compared with some more opened network notions such as Quality of Service or VLAN. The network switching technology, associated with the full-duplex links, and the reserved bandwidth mechanism, eliminates all of the collisions.

In particular, AFDX uses new addressing and scheduling policies within a global network partition, which is based on the definition of the Virtual Links, or simply VL.

Each VL is a kind of communication channel, defined as a partition of the switched AFDX network, with a well defined transmission time fragmentation, which guarantees:

- Reserved path into the switched network topology from one source to a fixed number of destinations
- Reserved bandwidth into the global AFDX network
- Global time scheduling between asynchronized End Systems
- Known maximum latencies and jitters
- Access delay to the network
- End-to-end delivery, without acknowledgements nor retries

The bandwidth control is achieved by the timing constraints associated to each VL. The mapping of the VL into the global switched network realizes a partitioning of the topology, each VL has an associated time fragmentation called BAG (Bandwidth Allocation Gap) and a maximum frame size. The BAG associated to each VL is the precise time unit between 2 consecutive IP frames sent by the End System.

The VLs with the same BAG are therefore aggregated into fixed time slots, which guarantee the maximum jitter of the transmission. The BAG also defines the maximum delay for the transmission of each frame.

The switch knows which VLs and which frames to connect by a means of static configurable table.

5.0 CES Building Block Modules (HW & SW) used in CES AFDX solution

The product strategy development has aimed the following main points:

- i. Design the AFDX modules anticipating as much as possible any enhancement, new requirements from AFDX specification authority e.g. Airbus
- ii. Capability to build test system for various architectures and various environments
- iii. Re-use of the generic architecture used in CES catalogue products across vertical markets. The AFDX hardware and software modules are based on the elements described in the following pages. No special hardware is added except the specific electrical interface (Specific to a given avionics bus). Software framework is split between hardware modules in a way to make use of this CES generic architecture and building blocks.
- iv. Offer a bundle configuration Hardware and Software packaged together

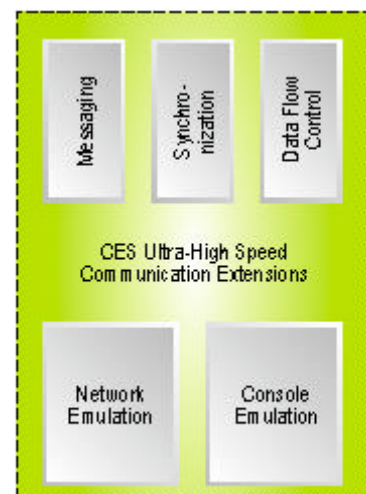
5.1 Hardware Elements

A. VME PROCESSOR BOARD

The architecture of the PowerPC-based RIO3 8064 is depicted in the figure 6.

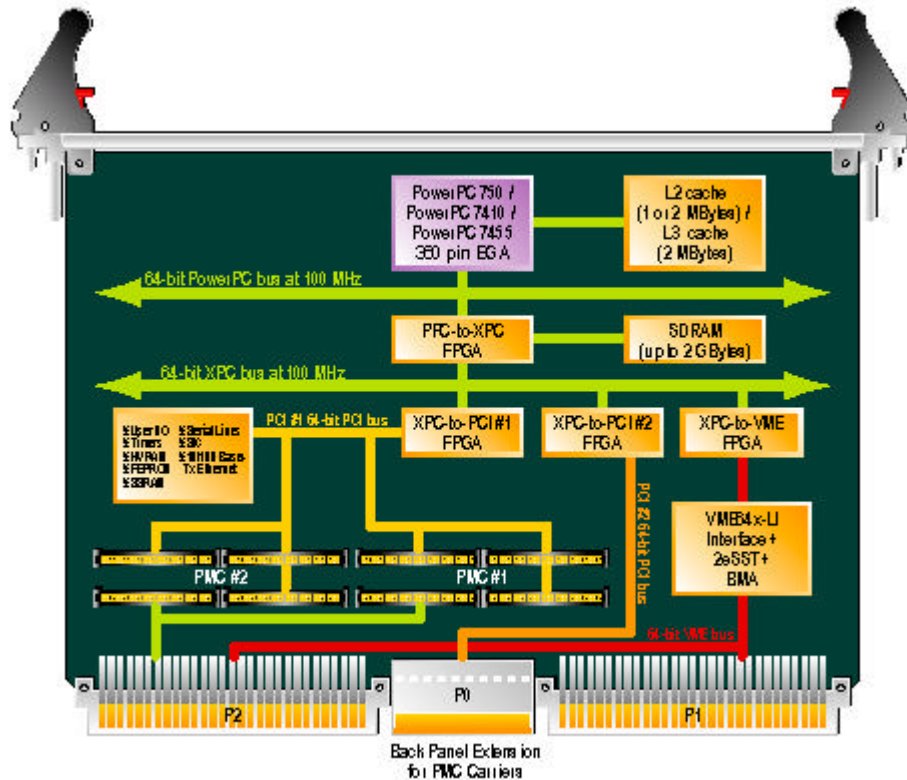
The CES RIO3 PCI interface logic incorporates special features allowing ultra high speed communication between the MFCCs (PMC daughter cards plugged on the RIO3). The VME processor offers the following features:

- **Brute Force Power.** PowerPC 750 with 1 MByte external L2 cache, PowerPC 7410 with 1 or 2 MBytes external L2 cache, or PowerPC 7455 with 2 MBytes external L3 cache
- Global Memory at Cache Speed
- Three concurrent buses at full speed (2 x 64-bit PCI and 1 x 64-bit VME64x-LI / CompactPCI)
- CES-designed direct PowerPC-to-PCI bridges
- Optimized bus architecture for maximum bus bandwidth
- Multiple arbiters for memory bandwidth allocation
- Two onboard dual PMC slots
- Supports up to six AFDX PMCs with OMC extension boards



The back-end PowerPC runs a real time operating system hosts the AFDX drivers and the API library, providing the user with access to the full set of AFDX services for each of the onboard AFDX PMCs.

Figure 6 Architecture of the CES RIO3 8064



B. AFDX PMCs

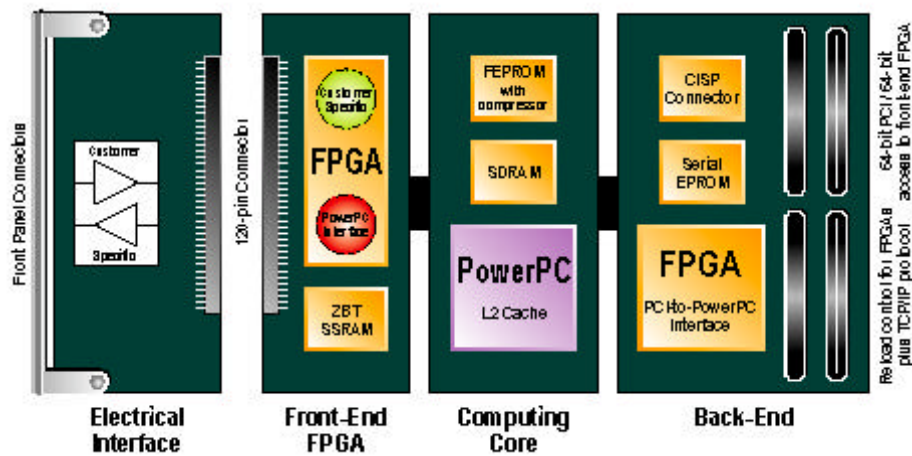
The architecture of the PowerPC based MFCC 8443 is summarized in the figure 5.3. The MFCC 8443 uses processor IBM 750Cxe with an ultra high speed front end FPGA to powerPC memory coupler, equipped with a dual ported memory multiple buffer and bi-directional FIFOs. The AFDX PMCs has the features of the MFCC family product:

- PPMC compliant
- IBM 750CSe computing core at 600 MHz
- 600 KGates user-specific FPGA directly coupled with the PowerPC memory through the CES FPGA-PowerPC ultra-high-speed interface
- 64-bit PCI master / slave with CES messaging mechanism
- 72-bit front and 64-bit rear access for user I/O
- User FPGA development toolkit
- High performance VxWorks® and LynxOS® BSPs with multiprocessor support

The use of the AFDX mechanism is as follows:

- The electrical interface hosts the Ethernet physical interfaces and the connectors.
- The front-end FPGA hosts all of the hardware-critical functional blocks, such as the hardware trigger functions, time-stamping, specific AFDX MACs.
- The dedicated PowerPC runs a real-time operating system and takes care of the End System definition, handles all of the specified AFDX services (Tx / Rx, client class, MIB, traffic shaping, redundant management, sampling, queuing) and additional functions used in a test environment such as error injection, low-level frame monitoring.

Figure 7 Architecture of the CES MFCC 8443



Inherent to the AFDX functionality, we can outline the following capabilities.

AFDX NETWORK ANALYSIS

- Raw data acquisition, recording and analysis
- Snoop AFDX traffic with detailed reports
- Automatic traffic generation
- Full bandwidth simultaneous input capture and output generation flow
- Error injection capability (bad FCS/CRC, BAG violation, erroneous MAC or IP addresses, SN errors, etc.)
- Error analysis and statistics
- High-level user interface
- Time-stamping with 1 micro second precision
- Multiple event composition filtering and triggering

AFDX END SYSTEM CONNECTION

CES products provide a data communication API, which guarantees the correct use of AFDX, for real-time user application based on AFDX:

- Configuration table control
- VL, sub VL and BAG control
- Errors analysis and statistics
- Redundancy management
- User-application interface for multiple avionics equipment simulation (ARINC 653 APEX definition compliant)
- Queuing and sampling ports for VL access
- Per VL statistic information
- IP, UDP and ICMP protocols
- SAP (Service Access Point) interface
- Time-stamping with 1 μ s precision
- Multiple end-system emulation

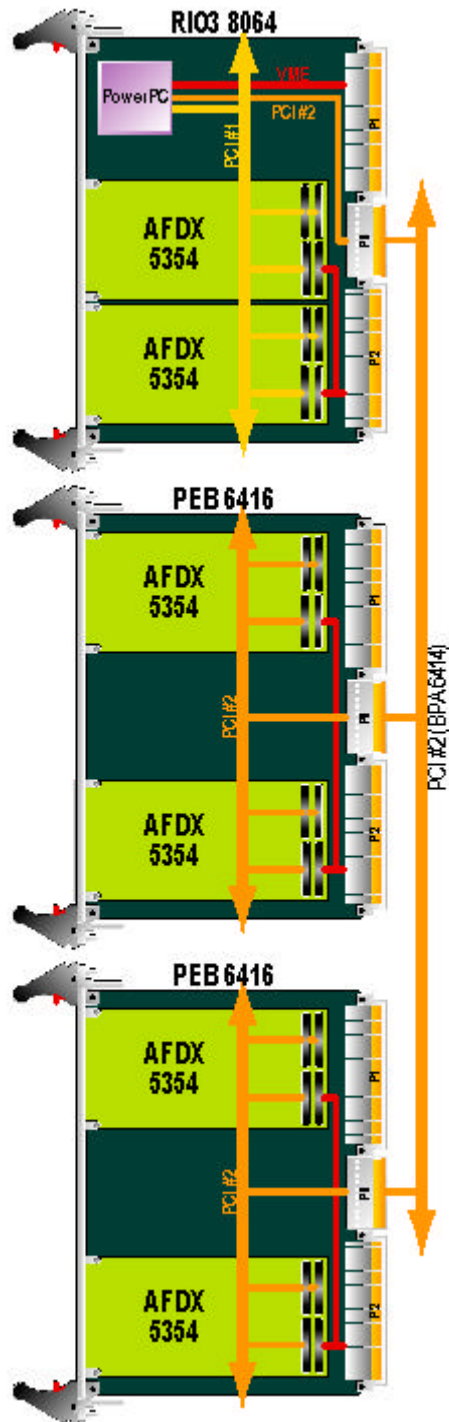
For performance reason, most of the functions listed below have been developed and coded in firmware. The CES products provide both high level services and low level controls for protocol analysis.

Electrical interface is designed for multiple Tx, multiple Rx, combined Tx/Rx application Components selected for the electrical interface allowed the use of the AFDX PMC for ruggedized applications (e.g. flight test).

C. PEB (PMC EXTENSION BOARD)

The PEB module allows extension possibilities from a basic configuration.

Figure 8 PEB / AFDX



ADDING AFDX CHANNELS (INPUT)

It is possible to increase the number of AFDX PMCs controlled by the master CPU carrier by adding one or two PMC extension boards (PEB 6416) which are connected to the second PCI bus of the RIO3 8064.

One RIO3 can drive up to 6 PMCs offering the possibility to generate an AFDX cluster (12 AFDX channels) or to mix AFDX with other types of interfaces e.g. network interface, other type of avionics bus) in a cost efficient manner.

The various MFCCs are located on the PEBs which are connected to the second PCI bus of the RIO3 8064.

5.2 Software Elements

A layered framework of software supports the hardware elements and the distribution chosen is described in Figure 9. The end User develops its application in using validated call functions accessible in the AFDX service library. The library calls the AFDX driver and the driver calls the firmware which resides on the AFDX PMC.

End user has then access to configuration set up, mode of operations in Tx and Rx, statistics, error detection and injection hardware, filter and trigger.

To address and satisfy the performance issue, concurrent design was establish between the Software engineering team and the firmware engineering team.

Figure 9 User Software Interface

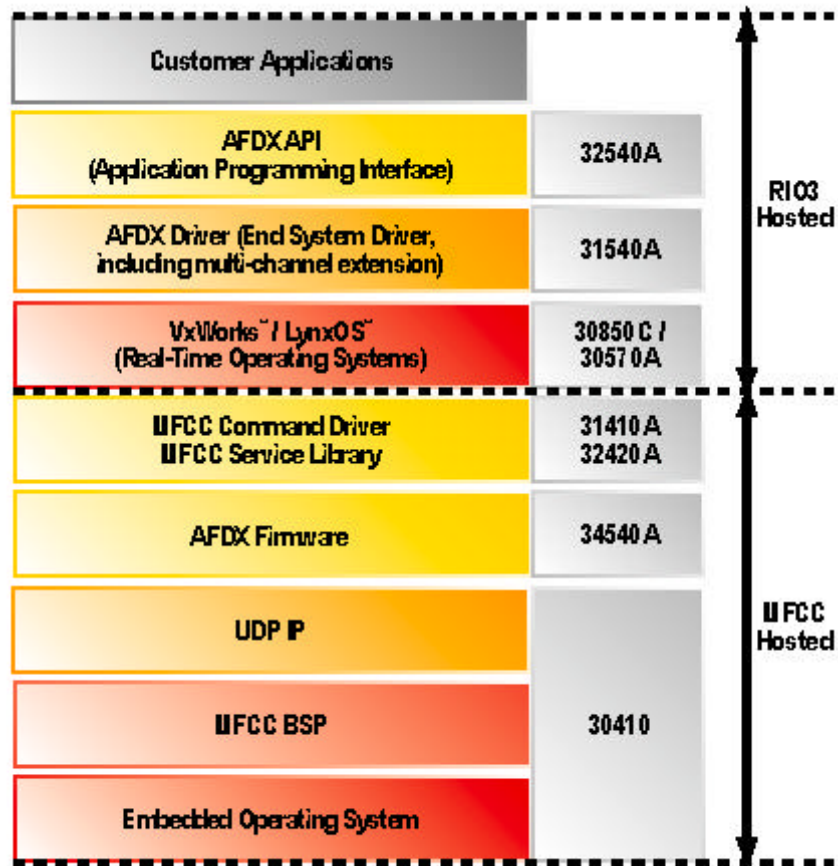
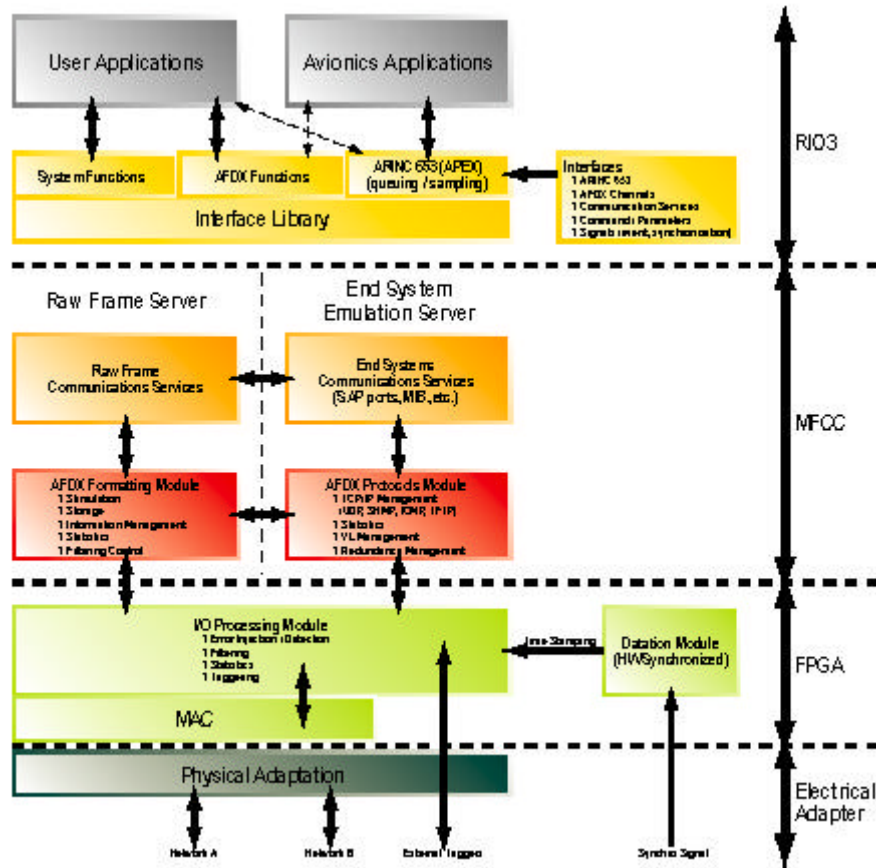


Figure 10 summarizes how end user can access the different AFDX services and the operations modes with a bundle 8854.

Figure 10 Organization Design of AFDX Software and Firmware



5.3 The CES AFDX Bundle

The bundle configuration allows end user to develop their application with a minimum of risk and development time. As depicted by Figure 9, CES can deliver the hardware and Software elements packaged together and ready to use. The ultimate benefit for end users are protection of its software application by a means of obsolescence management plan incorporated in a specific quality plan and version control. Remote reconfiguration capability can also be proposed as part of CES on line support (Programmable hardware elements, firmware, OS, application via network facilities). In CES terminology one bundle is one combination of hardware elements with one combination of software elements

Table 2 MIL-1553 Interface (Example 1)

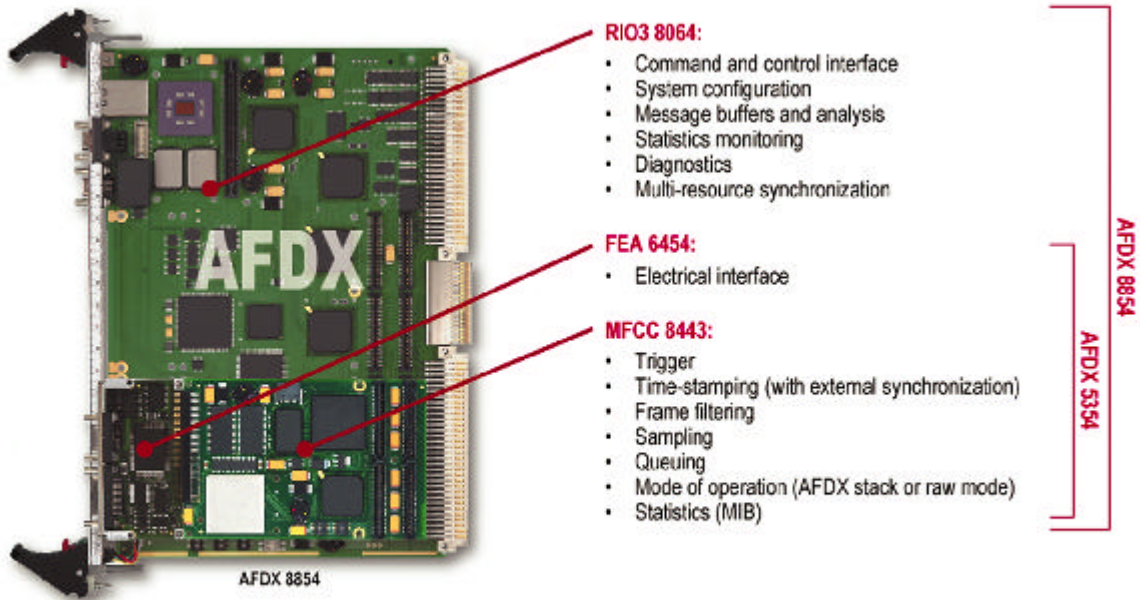
Part Number Bundle	Part Number of Bundle Elements
Homologated Bundle 8753AB for MIL-1553 Interface	8064DB: RIO3 8064
	5364CA: MIL1553B
	6064AO: MIL 1553B Signal Conditioning Unit
	3057D: VxWorks 5.4 for RIO3 8064
	3141B: MFCC Command Driver
	32420B: MFCC service library
	31530B: Vxworks driver for 1553 PMC

Table 3 AFDX Interface (Example 2)

Part Number Bundle	Part Number of Bundle Elements
Homologated Bundle 8854DA for AFDX Interface	8064DB: RIO3 8064DB
	5354BA: Two PMCs AFDX
	30570D: VxWorks 5.4 for RIO3 8064
	32540B: AFDX API LIBRARY
	31540B: AFDX DRIVER

One of the last key features available on the AFDX PMC is the possibility to use the PMC as a multi end system emulator. Main benefit for end users is the optimization of the hardware count.

Figure 11 AFDX Bundle Hardware Topology



5.4 Part Number for CES AFDX Products

5354BA	PMC-based AFDX LynxOS Interface
8064DB	RIO3
8854CA	AFDX LynxOS Bundle Package
8854DA	AFDX LynxOS Bundle Package
8854EA	AFDX VxWorks Bundle Package
36540A	AFDX Command Interface for VME
36540B	AFDX Command Interface for CPCI
36540C	AFDX Command Interface for Ethernet
6461A0	PMC Extension Board for VME Processor RIO3

6.0 Possible Types of Architectures Test System with CES AFDX Modules

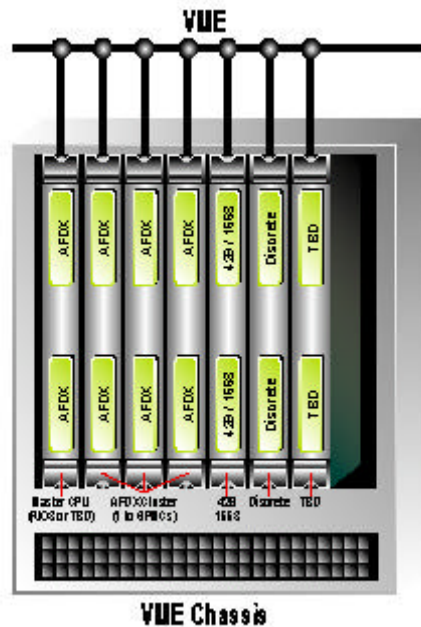
Using the hardware and software described in section 5.0, end user can implement various architectures for their test systems. In addition to board level supplier, CES has the capability to deliver complete validated and tested sub system when requested by customers. CES then performs integration tasks leading to the delivery of a turnkey solution.

6.1 Different Types of Architecture

Subject to level of performance required and the level of legacy related to previous test bench development, end user has the capability to develop their application on a workstation or a master CPU (TDB) or the RIO3 itself. When third party CPU is used, a RIO3 is viewed as a device.

The AFDX PMC is compatible with the other PMCs in the CES aerospace family (MIL-STD-1553, Datation, etc). The use of PEB (PCI multi processor extension) allows for multiple AFDX PMCs to be handled by one processor (one RIO3). Figure 12 describes the architecture in this case.

Figure 12 AFDX Interface in Cluster associated with other type of interfaces (Example of VME System Architecture)



As PEBs also allowed one AFDX PMC to be handled by multiple processors, users can build client/servers type topologies.

TYPICAL ARCHITECTURE

a. dev on RIO3 (on top of service library)

b. black box

The VME command interface (AFDX protocol converter) is a server running on the RIO3 host. It handles communication between the outside world and the CES AFDX cluster hosted on the RIO3. Once the server is running, external applications shall post requests through the VME interface of the RIO3. Basically application requests are converted to function calls to the AFDX library.

As this protocol converter module is OS independent, that offers end users further flexibility for their application.

c. AFDX Software Analyzer



The AFDX Software Analyzer is available on both VME and CPCI CES boards.

6.2 Portable AFDX Analyzer - Standalone Tool - CAD-X Software Analyzer

Using the same building block modules described in section 5.0, users have the possibility to build a standalone tool. Figure 13 describes the architecture and principles. A set of menus and pop up windowing allow users to manage the following functions:

- System configuration,
- Filtering and trigger Set up
- Terminal set up
- Scenario definition
- Operation mode
- Status Control
- Journaling
- Import/ Export set up
- Interface to external database and generation of configuration table (AFDX mode stack)
- Configuration table checking and bandwidth usage calculation



Further details can be found in the datasheet *CAD-X AFDX Software Analyzer*.

Figure 13 CAD-X / AFDX Software Analyzer

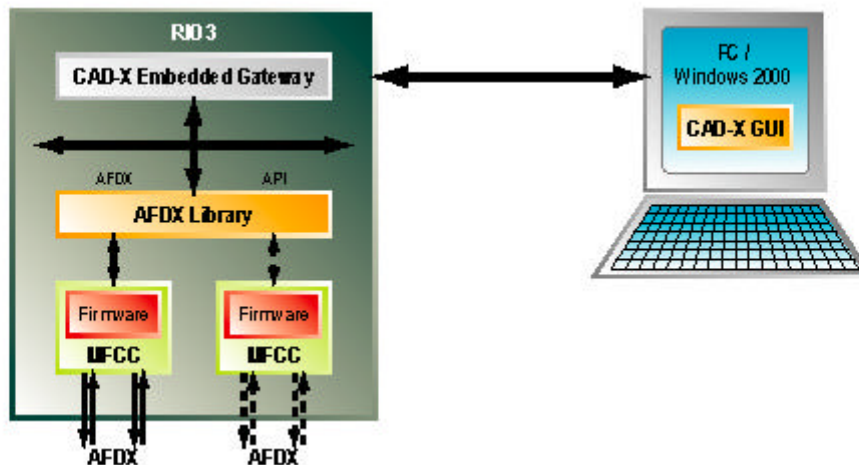


Figure 14 CAD-X System



7.0 Beyond the Airbus A380 Program and Current Standardization Effort

The AFDX concept and IMA architecture has introduced for the first time network technology in avionics systems. Specifications have provided the AFDX with the required deterministic performance. The plan is now to capitalize on such effort and introduce AFDX in other aircraft program in the near future (new aircraft and major retrofit).

Evolution of the CES AFDX resources will be easy to make taking into account the design and validation effort performed in the early stage of the project. Enhancements, e.g. additional functionality can be added without complete re design of the AFDX PMC. For a given set of functions, technology insertion will lead as well to cost reduction for future AFDX projects.

In term of support through the A380 life cycle, CES has put in place a specific plan of warranty and maintenance with Airbus. Such a plan has satisfied Airbus obsolescence management requirements.

The increased interest of the civil aerospace community for technology used in non avionics business led in the late 90s to the inception of the ADN (Aircraft Data Network) Working Group under the umbrella of ARINC. The goal of the ADN working group is to work on the adoption of existing network standards to an aircraft environment. The tasks for the last past years have been to establish/specify standardization of Ethernet communications technology for use in aircraft avionics systems. This initiative entitled project paper 664" is composed of various parts. Each part deals with a specific task/topic:

- Part 1: System concept (Architecture and Topology)
- Part 2: Ethernet Physical and datalink layer specification
- Part 3: Internet based protocols
- Part 4: Internet based Address Structure
- Part 5: Network Interconnection Services and Functional Elements
- Part 6: Network management
- Part 7: Deterministic Network

Part 7 considers an example of deterministic network and the current and informative example reviewed is based upon an AFDX network. Since 2002, Airbus and other companies participated in a review for Draft 1 of Project Paper 664, part 7.